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EXAMINER	
CHENG, PETER L	
ART UNIT	**PAPER NUMBER**
2609	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/726,657	CHANG ET AL.	
	Examiner	Art Unit	
	Peter L. Cheng	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because:

- **Fig. 5, steps 71 through 74** contain grammatical errors; in **step 73**, **required** is misspelled as **reguired**; the following are only suggestions:

  Step 71: Send a color index to the cache;

  Step 72: Determine if matching color information exists in the cache; if so, go to step 74; otherwise, go to step 73;

  Step 73: Load the cache with the required color information from a color table;

  Step 74: Return the color information which corresponds to the color index;

- **Fig. 5:** the direction of the arrow between **step 72** and **step 73** should be reversed; that is, it should be pointing to the right;

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be

canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities:

- There are some typographical and grammatical errors in the disclosure; for example, **page 1, line 11** ("*in associated* with the progress ..."), **page 1, line 30** ("more vibrant color *image*"), **page 2, lines 23 – 24** ("that the color processor 11 and the color table 2 respectively *is* connected ..."), **page 3, line 20** ("*aforementionedgoals*"), **page 5, line 1** ("which *is coupled* the color processor ..."), **page 5, line 22** ("if so, *goes* to step 74; if not, *goes* to step 74"), **page 5, line 25** ("available in the cache 52 or *not?*"), **page 6, line 4** ("will be *send* back ..."), **page 6, line 13** ("*have* direct impact"), **page 6, line 18**

("*overgreat* memory"), **page 6, lines 18 – 19** ("but *the wastes of precious area* is not the outcome ..."),

- **Page 6, lines 11, 14:** it is assumed that applicant intended to cite **size of the cache** instead of **number of the cache**;

Appropriate correction is required.

Claim Objections

3. Claim 2 is objected to because of the following informalities:
   - **Page 8, line 14:** it is assumed that applicant intended to cite "**are in different devices**" instead of "**are in *the* different devices**";

4. Claim 10 is objected to because of the following informalities:
   - **Page 9, line 28:** it is assumed that applicant intended to cite "**are in different devices**" instead of "**are in *the* different devices**";

5. Claim 11 is objected to because of the following informalities:

- **Page 9, line 31:** it is assumed that applicant intended to cite "**a portion of the color data similar to the corresponding color data is**" instead of "**a portion of the color data similar to the corresponding color data are**";

Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1 – 12 are rejected under 35 U.S.C. 102(b) as being anticipated by **Gibson (US Patent 6,246,396 B1).**

As for claim 1, GIBSON teaches a method for color processing realized by a color processing apparatus, which comprises

a color table for storing a plurality of color data [Gibson cites the use of external memory for storing this color data. "These 8 different addresses designate the location of the 8 output color values CV(P0) – CV(P7) in the respective memory banks **573** (FIG. 62) of the data cache **230** (FIG. 2)"; **col. 51, lines 59 – 62.** "If the 2 bit tag does not correspond to the two most significant

bits of the 9 bit addresses, then the output color values CV(P0) – CV(P7) do not exist in the cache memory **230.** Hence, in step S7, all the output color values corresponding to the 2 bit tag entry for that line are read from external memory into the data cache **230**"; **col. 52, lines 3 - 9],**

and a cache memory for caching part of the color data [Fig. 2, data cache **230],**

the method comprising the steps of:

issuing a color index ["In operation, one or both of the operand organizers **247** or **248** (FIG. 2) supplies an index **1874** and asserts a data request signal **1876**"; **col. 104, lines 20 - 22];**

returning at least one of the color data corresponding to the color index if the at least one of the color data is cached in the cache memory ["If the requested data is present in cache memory **230,** an acknowledgment signal **1879** is supplied to the relevant operand organizer **247** or **248** together with the requested data **1880**"; **col. 104, lines 29 - 32];**

and returning at least one of the color data from the color table if the at least one of the color data is not cached in the cache memory ["If the requested data is not present in the cache **230,** the requested data **1870** is

fetched from external memory, via an input bus interface **1871** and the input interface switch **252** (FIG. 2). The data **1870** is fetched by asserting a request signal **1882** and supplying the generated address(es) **1877** of the requested data **1870.** An acknowledgment signal **1883** and the requested data **1870** are then sent to the cache controller **1878** and the cache memory **230** respectively. The relevant cache-line(s) of the cache memory **230** are then updated with the new data **1870**"; **col. 104, lines 32 - 41].**

Regarding claim 2, GIBSON further teaches the method for color processing of claim 1,

wherein the color table and the cache memory are in the different devices [As previously noted for claim 1, Gibson cites the use of external memory for storing this color data. "If the 2 bit tag does not correspond to the two most significant bits of the 9 bit addresses, then the output color values CV(P0) – CV(P7) do not exist in the cache memory **230.** Hence, in step S7, all the output color values corresponding to the 2 bit tag entry for that line are read from external memory into the data cache **230**"; **col. 52, lines 3 - 9].**

Regarding claim 3, GIBSON further teaches the method for color processing of claim 1, further comprising:

writing the at least one of the color data corresponding to the color index into the cache memory from the color table if the at least one of color data is <u>not</u> cached in the cache memory [As previously noted for claim 1, "If

the requested data is not present in the cache **230,** the requested data **1870** is fetched from external memory, via an input bus interface **1871** and the input interface switch **252** (FIG. 2). The data **1870** is fetched by asserting a request signal **1882** and supplying the generated address(es) **1877** of the requested data **1870.** An acknowledgment signal **1883** and the requested data **1870** are then sent to the cache controller **1878** and the cache memory **230** respectively. The relevant cache-line(s) of the cache memory **230** are then updated with the new data **1870**"; **col. 104, lines 32 - 41].**

Regarding claim 4, GIBSON further teaches the method for color processing of claim 3, further comprising:

writing a portion of the color data *similar* to the at least one of the color data corresponding to the color index into the cache memory from the color table if the at least one of the color data corresponding to the color index is not cached in the cache memory [Gibson teaches that an objective of the cache memory is to contain "the eight output color values CV(P0) – CV(P7) surrounding the input pixel"; **col. 52, lines 13 – 14.** These eight color values are similar to the color that corresponds to the color index (that is, the "input pixel"). "If the 2 bit tag does not correspond to the two most significant bits of the 9 bit addresses, then the output color values CV(P0) – CV(P7) do not exist in the cache memory **230.** Hence, in step S7, all the output color values corresponding to the 2 bit tag entry for that line are read from external memory

into the data cache **230**"; **col. 52, lines 3 - 9].**

Regarding claim 5, GIBSON further teaches an apparatus for color processing, comprising:

a memory for storing at least a color table comprising a plurality of color data [As previously noted for claim 1, Gibson cites the use of external memory for storing this color data. "These 8 different addresses designate the location of the 8 output color values CV(P0) – CV(P7) in the respective memory banks **573** (FIG. 62) of the data cache **230** (FIG. 2)"; **col. 51, lines 59 – 62.** "If the 2 bit tag does not correspond to the two most significant bits of the 9 bit addresses, then the output color values CV(P0) – CV(P7) do not exist in the cache memory **230.** Hence, in step S7, all the output color values corresponding to the 2 bit tag entry for that line are read from external memory into the data cache **230**"; **col. 52, lines 3 - 9]; and**

a color processing module coupled to the memory, comprising:
a cache for storing at least one of the color data selected from the color table [Fig 1, cache **230]; and**

a color processor, coupled to the cache, for performing color conversions and operations [Fig. 1, host CPU **202** is coupled to the cache via the PCI bus interfaces **207** and **221];**

wherein the color processor issues a color index to search for a corresponding color data from the cache, and the corresponding color data is loaded from the color table into the cache if the corresponding color data is not found in the cache [From **Fig. 4,** Gibson illustrates the control of the co-processor **224** by the color processor (that is, CPU **202**) by means of an instruction queue **1022.** Operand **1023** is acted upon by co-processor **224** by either operand organizer B (**Fig. 2, 247**) or operand organizer C (**Fig. 2, 248**). As noted previously for claim 1, "In operation, one or both of the operand organizers **247** or **248** (FIG. 2) supplies an index **1874** and asserts a data request signal **1876**"; **col. 104, lines 20 – 22.** "If the requested data is not present in the cache **230,** the requested data **1870** is fetched from external memory, via an input bus interface **1871** and the input interface switch **252** (FIG. 2). The data **1870** is fetched by asserting a request signal **1882** and supplying the generated address(es) **1877** of the requested data **1870.** An acknowledgment signal **1883** and the requested data **1870** are then sent to the cache controller **1878** and the cache memory **230** respectively. The relevant cache-line(s) of the cache memory **230** are then updated with the new data **1870**"; **col. 104, lines 32 - 41].**

Regarding claim 6, GIBSON further teaches the apparatus for color processing of claim 5,

wherein the memory is independent of the cache [As previously noted for claim 1, Gibson cites the use of external memory for storing color data. "If the 2 bit tag does not correspond to the two most significant bits of the 9 bit addresses, then the output color values CV(P0) – CV(P7) do not exist in the cache memory **230.** Hence, in step S7, all the output color values corresponding to the 2 bit tag entry for that line are read from external memory into the data cache **230**"; **col. 52, lines 3 - 9].**

Regarding claim 7, GIBSON further teaches the apparatus for color processing of claim 5,

wherein, while the corresponding color data is loaded from the memory into the cache, a portion of the color data similar to the corresponding color data are also loaded into the cache [As previously noted for claim 4, Gibson teaches that an objective of the cache memory is to contain "the eight output color values CV(P0) – CV(P7) surrounding the input pixel"; **col. 52, lines 13 – 14.** These eight color values are similar to the color that corresponds to the color index (that is, the "input pixel"). "If the 2 bit tag does not correspond to the two most significant bits of the 9 bit addresses, then the output color values CV(P0) – CV(P7) do not exist in the cache memory 230. Hence, in step S7, all the output color values corresponding to the 2 bit tag entry for that line are read from external memory into the data cache 230"; **col. 52, lines 3 - 9].**

Regarding claim 8, GIBSON further teaches the apparatus for color processing of claim 5, wherein the cache comprises:

> **a cache controller [Fig. 141,** cache controller **1878], coupled to the memory, for loading the corresponding one of the color data from the memory into the cache if the corresponding color data is not found in the cache [**"If the requested data is not present in the cache **230,** the requested data **1870** is fetched from external memory, via an input bus interface **1871** and the input interface switch **252** (FIG. 2). The data **1870** is fetched by asserting a request signal **1882** and supplying the generated address(es) **1877** of the requested data **1870.** An acknowledgment signal **1883** and the requested data **1870** are then sent to the cache controller **1878** and the cache memory **230** respectively. The relevant cache-line(s) of the cache memory **230** are then updated with the new data **1870**"; **col. 104, lines 32 - 41].**

Regarding claim 9, GIBSON further teaches an apparatus for accelerating color processing coupled to an external color table storing a plurality of color data, comprising:

> **a color processor performing color conversions and operations [Fig. 1,** host CPU **202** is coupled to the cache via the PCI bus interfaces **207** and **221]; and**
>
> **a cache coupling the color table and the color processor and storing at least one of the color data selected from the color table [Fig 1,** cache

230];

wherein the color processor issues a color index to search for a corresponding color data from the cache, and the corresponding color data is loaded from the color table into the cache if the corresponding one of the color data is not found in the cache [From **Fig. 4,** Gibson illustrates the control of the co-processor **224** by the color processor (that is, CPU **202**) by means of an instruction queue **1022.** Operand **1023** is acted upon by co-processor **224** by either operand organizer B (**Fig. 2, 247**) or operand organizer C (**Fig. 2, 248**). As noted previously for claim 1, "In operation, one or both of the operand organizers **247** or **248** (FIG. 2) supplies an index **1874** and asserts a data request signal **1876**"; **col. 104, lines 20 – 22.** "If the requested data is not present in the cache **230,** the requested data **1870** is fetched from external memory, via an input bus interface **1871** and the input interface switch **252** (FIG. 2). The data **1870** is fetched by asserting a request signal **1882** and supplying the generated address(es) **1877** of the requested data **1870.** An acknowledgment signal **1883** and the requested data **1870** are then sent to the cache controller **1878** and the cache memory **230** respectively. The relevant cache-line(s) of the cache memory **230** are then updated with the new data **1870**"; **col. 104, lines 32 - 41].**

Regarding claim 10, GIBSON further teaches the apparatus for accelerating color

processing of claim 9,

wherein the color table and the cache memory are in the different devices [As previously noted for claim 1, Gibson cites the use of external memory for storing color data. "If the 2 bit tag does not correspond to the two most significant bits of the 9 bit addresses, then the output color values CV(P0) – CV(P7) do not exist in the cache memory **230.** Hence, in step S7, all the output color values corresponding to the 2 bit tag entry for that line are read from external memory into the data cache **230**"; **col. 52, lines 3 - 9].**

Regarding claim 11, GIBSON further teaches the apparatus for accelerating color processing of claim 9, wherein,

while the corresponding color data is loaded from the color table into the cache, a portion of the color data similar to the corresponding color data are also loaded into the cache [As previously noted for claim 4, Gibson teaches that an objective of the cache memory is to contain "the eight output color values CV(P0) – CV(P7) surrounding the input pixel"; **col. 52, lines 13 – 14**. These eight color values are similar to the color that corresponds to the color index (that is, the "input pixel"). "If the 2 bit tag does not correspond to the two most significant bits of the 9 bit addresses, then the output color values CV(P0) – CV(P7) do not exist in the cache memory 230. Hence, in step S7, all the output color values corresponding to the 2 bit tag entry for that line are read from external memory into the data cache 230"; **col. 52, lines 3 - 9].**

Regarding claim 12, GIBSON further teaches the apparatus for accelerating color processing of claim 9, wherein the cache further comprises:

> **a cache controller [Fig. 141,** cache controller **1878], coupled to the color table, for loading the corresponding color data from the color table into the cache if the corresponding color data is not found in the cache [**"If the requested data is not present in the cache **230,** the requested data **1870** is fetched from external memory, via an input bus interface **1871** and the input interface switch **252** (FIG. 2). The data **1870** is fetched by asserting a request signal **1882** and supplying the generated address(es) **1877** of the requested data **1870.** An acknowledgment signal **1883** and the requested data **1870** are then sent to the cache controller **1878** and the cache memory **230** respectively. The relevant cache-line(s) of the cache memory **230** are then updated with the new data **1870**"; **col. 104, lines 32 - 41].**

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Peter L. Cheng whose telephone number is 571-270-3007. The examiner can normally be reached on MONDAY - FRIDAY, 8:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Chris Kelley can be reached on 571-272-7331. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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